REMARKS

Claims 1-15 are pending in the application with claims 1, 7, and 10 amended herein. No amendment made was related to the statutory requirements of patentability. All amendments made herein now more positively express limitations that were previously inherent in such claims and, accordingly, are not for the purpose of narrowing and do not effectively narrow the scope of any claim.

Claims 1-15 stand rejected under 35 USC 103(a) as being unpatentable over Chi in view of Raaijmakers. Applicants request reconsideration.

Amended claim 1 sets forth a capacitor fabrication method that includes, among other features, forming a first capacitor electrode comprising TiN over a substrate, forming a capacitor dielectric layer over the first electrode, and forming a second capacitor electrode over the dielectric layer. The first capacitor electrode has an innermost surface area per unit area and an outermost surface area per unit area that are both greater than an outer surface area of the substrate. Page 3 of the Office Action admits that Chi does not disclose or suggest a first capacitor electrode comprising TiN, as set forth in claim 1. Instead, Chi states in col. 3, lns. 15-18 that the first electrode includes heavily doped polysilicon. Page 3 of the Office Action relies on Raaijmakers as allegedly disclosing a TiN bottom electrode in paragraph [0013]. Thorough review of the referenced text of Raaijmakers as well as the remaining text reveals that Raaijmakers does not disclose the alleged teaching.

Paragraph [0013] of Raaijmakers does not provide any mention of bottom electrode 22 or 42 comprising TiN. Bottom electrodes are consistently described throughout Raaijmakers as containing silicon without indicating any alternative materials (Abstract,

Ins. 1-3; para. [0020], Ins. 7-9; para. [0040], Ins. 1-4). Rather, it is entirely clear from Raaijmakers, as stated in the Abstract and elsewhere, that bottom electrodes 22 and 42 are required to contain silicon since the entire purpose of the invention involves formation of conformal dielectrics over "textured silicon electrodes." The only disclosure or suggestion of TiN in Raaijmakers is a barrier layer formed over the capacitor dielectric and comprised by the top electrode, as discussed in paras. [0132] to [0133].

Neither Chi nor Raaijmakers provide any disclosure or suggestion that TiN may be suitably used as the first electrode of claim 1. The allegation on page 3 of the Office Action is incorrect in stating that Raaijmakers discloses a TiN bottom electrode. No such disclosure exists. The Office Action does not allege that Chi or Raaijmakers somehow suggest the TiN barrier layer of Raaijmakers should instead be used as a bottom electrode. Applicants assert that Raaijmakers requires a textured silicon bottom electrode and cannot be considered to provide such a suggestion. Also, Applicants assert that Chi does not provide any such suggestion.

Rather, the only suggestion is in the Applicants' own specification describing a first capacitor electrode comprising TiN. Thus, it is clearly apparent that any rejection based on the currently cited art finding a suggestion to use TiN as a bottom electrode constitutes impermissible hindsight reconstruction using Applicants' own specification as a roadmap for guidance. Neither Chi nor Raaijmakers disclose or suggest a first capacitor electrode comprising TiN, as claimed. Accordingly, combination of the references cannot be considered to somehow provide a teaching that is absent from both. At least for such reason, claim 1 is patentable over Chi in view of Raaijmakers. Claims 2-9 depend from

claim 1 and are further patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested.

Claim 10 sets forth a capacitor fabrication method that includes, among other features, forming a layer of polysilicon over the sides and bottom of an opening in an insulative layer over a substrate, removing the polysilicon layer from over the bottom, and converting at least some of the polysilicon layer to hemispherical grain polysilicon. The method further includes forming a first capacitor electrode on the hemispherical grain polysilicon, forming a capacitor dielectric layer on the first electrode, and forming a second capacitor electrode over the dielectric layer. Pages 2-3 of the Office Action allege that Chi discloses the method of claim 10. However, Applicants assert that Chi does not disclose or suggest forming a first capacitor electrode "on the hemispherical grain polysilicon," as defined in claim 10.

Page 2 of the Office Action incorrectly states that Chi describes converting polysilicon layer 201 to HSG and forming electrode 301 "on the converted polysilicon." The converted polysilicon of claim 10 is clearly HSG polysilicon. The amendment herein to claim 10 reinforces the already inherent composition of the converted polysilicon by stating that the first capacitor electrode is formed ON the HSG polysilicon. By comparison, column 3, lines 4-19 of Chi clearly describe that HSG silicon nodules 203 and amorphous silicon sidewall spacers 201 are completely oxidized. That is, nodules 203 and spacers 201 are entirely converted to silicon dioxide. Accordingly, nodules 203 and spacers 201 do not contain HSG silicon or even amorphous silicon when the heavily doped polysilicon 301 is formed thereon. It is thus impossible for polysilicon 301 to be formed on HSG polysilicon since HSG silicon no longer exists in nodules 203 or even spacers 201.

Nowhere does Chi disclose or suggest that heavily doped polysilicon 301 can be formed on nodules 203 or spacers 201 while such features are still comprised of HSG silicon or amorphous silicon. Raaijmakers does not disclose or suggest and the Office Action does not allege that Raaijmakers discloses or suggests forming a first capacitor electrode on HSG polysilicon, as set forth in claim 10. Neither Chi nor Raaijmakers disclose or suggest such a feature of claim 10. Accordingly, combination of the references cannot be considered to somehow provide a teaching that is absent from both. At least for such reason, claim 10 is patentable over Chi in view of Raaijmakers.

Claims 11-15 depend from claim 10 and are further patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested. For example, claim 14 sets forth that the first electrode comprises TiN. Page 3 of the Office Action admits that Chi does not disclose or suggest TiN as a first electrode. Also, as described above, Raaijmakers cannot be considered to provide such disclosure or suggestion either. Thus, claim 14 is further patentable over the cited art.

Applicants previously asserted in the prior response to the December 5, 2001 Office Action that Chi does not disclose or suggest forming a first capacitor electrode on HSG polysilicon. Even so, the Office Action does not provide any reply to the Applicants' prior assertion and merely repeats the previous incorrect allegation without any justification. Accordingly, the present Office Action is incomplete at least for such reason.

Further, as indicated above, all amendments made herein now more positively express limitations that were previously inherent in such claims. Since the meaning of the claims has not changed, but has merely been accentuated to the Office, the Office cannot find that any new ground of rejection was necessitated by the Applicants' amendments.

The claims as now constituted were previously before the Office and any new ground of rejection must be presented in a non-final rejection. Applicants respectfully request, if the Office disagrees with this just stated position, that the Office provided a well-reasoned justification for nevertheless making the next Office Action final.

At least for the reasons described herein, Applicants assert that all of claims 1-15 are in condition for allowance. Applicants request allowance of such claims in the next Office Action.

Applicants previously submitted Information Disclosure Statements dated August 16, 2001 and May 8, 2002 for which an initialed copy of the accompanying Form PTO-1449 has not yet been received. Applicants request review of the references cited therein and return of an initialed copy of the appropriate Form PTO-1449 indicating the same. If a copy of the initialed forms was already provided, then Applicants respectfully request a second copy since the forms were not received.

Respectfully submitted,

Dated: 12 Aug 2002 By: _____

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Application Serial No. 09/653,156
Filing Date ..... August 31, 2000
Inventor ..... Vishnu K. Agarwal, et al
Assignee ..... Micron Technology, Inc.
Group Art Unit 2813
Examiner ..... Y. Huynh
Attorney's Docket No. MI22-1518
Title: Capacitor Fabrication Methods

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO MAY 10, 2001 OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

1. (twice amended) A capacitor fabrication method comprising:

forming a first capacitor electrode comprising TiN over a substrate, the first electrode having an ~~inner~~ innermost surface area per unit area and an ~~outer~~ outermost surface area per unit area that are both greater than an outer surface area per unit area of the substrate;

forming a capacitor dielectric layer over the first electrode; and

forming a second capacitor electrode over the dielectric layer.

7. (once amended) The method of claim 1 wherein the ~~outer~~ outermost surface area of the first electrode is at least 30% greater than the outer surface area of the substrate.

10. (once amended) A capacitor fabrication method comprising:

forming an opening in an insulative layer over a substrate, the opening having sides and a bottom;

forming a layer of polysilicon over the sides and bottom of the opening;

removing the polysilicon layer from over the bottom of the opening;

converting at least some of the polysilicon layer to hemispherical grain polysilicon;

conformally forming a first capacitor electrode on the ~~converted~~ hemispherical grain polysilicon, the first electrode being sufficiently thin that the first electrode has an ~~outer~~ outermost surface area per unit area greater than an outer surface area per unit area of the substrate underlying the first electrode;

forming a capacitor dielectric layer on the first electrode; and

forming a second capacitor electrode over the dielectric layer.

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